

### **REMARKS**

Applicant thanks the Examiner for the thorough examination of the application. The title has been amended in accordance with the Examiner's suggestion. No new matter is believed to be added to the application by this amendment.

### **Status of the Claims**

Claims 1-3, 5, 8-16, 17, 18, 21 and 22-27 are pending in the application. The Examiner has withdrawn claims 8-16 and 23-27 from consideration. Support for the amendments to claims 1 and 17 can be found in Figure 13C and in paragraphs 52 and 53 of the specification. Claims 2 -7, 18, 20 and 21 have been amended to improve their language without decreasing their scope.

### **Objection to the Specification**

The Examiner has required a new title that indicates the subject matter being claimed. The Examiner's comments have been considered. The title has been amended in accordance with the Examiner's suggestion.

### **Rejection Under 35 U.S.C. §112, Second Paragraph**

Claim 17 is rejected under 35 U.S.C. §112, second paragraph as being indefinite. Applicant traverses.

Claim 17 has been amended to be clear, definite and have full antecedent basis. This rejection is accordingly overcome and withdrawal thereof is respectfully requested.

**Rejections under 35 U.S.C. §102(e) and §103(a)**

Claims 1, 2, 4, 5, 7 and 17-21 are rejected under 35 U.S.C. §102(e) as being anticipated by Yamazaki (U.S. Patent 6,323,528). The Examiner adds the teachings of Dimitrakopoulos (U.S. Patent 5,946,551) to rejected claim 3 under 35 U.S.C. §103(a). Applicant traverses.

The present invention pertains to a TFT substrate having an inverted-staggered type thin film transistor that finds a typical embodiment in claim 1:

1. A TFT array substrate for use in a liquid crystal display device, the TFT array substrate comprising:

a gate line arranged in a transverse direction over a substrate;

a metallic oxide layer surrounding the gate line;

a data line arranged in a longitudinal direction perpendicular to the gate line over the substrate;

a thin film transistor formed near the crossing of the gate and data lines, the thin film transistor comprising:

a gate electrode over the substrate, the gate electrode being extended from the gate line and surrounded by the metallic oxide so that the metallic oxide adheres to all faces of the gate electrode;

a gate insulation layer on the metallic oxide surrounding the gate electrode;

an active layer and an ohmic contact layer formed on the gate insulation layer;

a source electrode formed on the ohmic contact layer over the gate electrode and extended from the data line; and  
a drain electrode formed on the ohmic contact layer over the gate electrode and spaced apart from the source electrode;

a protection layer formed over said thin film transistor, the protection layer having a drain contact hole that exposes a portion of the drain electrode; and  
a pixel electrode formed in a pixel region that is defined by the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

An important aspect of the invention arises from the metallic oxide adhering to all faces of the gate electrode, as is shown in Figure 13C and 14C. This configuration helps prevent erosion and damage to the gate line and gate electrode, thereby preventing copper diffusion causing display defects.

Yamazaki is non-analogous art that pertains to a coplanar type thin film transistor. In Figures 3A-3G of Yamazaki, the coplanar type thin film transistor includes a gate electrode 25 or 26 over a silicon film 23 or 20. Also, the coplanar type thin film transistor of Yamazaki utilizes semi-amorphous silicon or a polycrystalline silicon for the silicon film.

In contrast, the Inverted-staggered type thin film transistor of the present invention includes active and ohmic contact layers (i.e., silicon layers) over the gate electrode, and the amorphous silicon is used for the active and ohmic contact layers. As a result, Yamazaki clearly fails to anticipate or suggest the claimed invention.

Moreover, Yamazaki discloses that the gate electrodes 25 and 26 were anodically oxidized to cover the surfaces thereof with aluminum oxide (see Yamazaki at column 12, lines 16-18). Therefore, the anodically oxidized film 40 only covers the exposed surfaces of the gate electrodes 25 and 26, as shown in FIG. 3E. In contrast, the metallic oxide layer of the present invention is formed by a thermal treatment, whereby the metallic oxide layer surrounds the whole surfaces of the gate electrode even the bottom surface. Figure 13C of the application shows the metallic oxide layer 112 adhering to all faces of the gate electrode 131. See instantly amended claims 1 and 17.

The Examiner turns to Dimitrakopoulos for teachings pertaining to copper. However, Dimitrakopoulos fails to address the failings of Yamazaki in disclosing or suggesting the claimed invention. The combination of Dimitrakopoulos with Yamazaki is therefore insufficient to allege *prima facie* obviousness over claims 3 and 22.

As a result, independent claims 1 and 17 are neither anticipated nor suggested by the applied prior art. Claims dependent upon claims 1 and 17 are patentable for at least the above reasons.

These rejections are accordingly overcome and withdrawal thereof are respectfully requested.

**Allowable Subject Matter**

The Examiner acknowledges the patentability of claim 6.

**Information Disclosure Statement**

Applicant thanks the Examiner for considering the Information Disclosure Statement filed October 16, 2002, and for making the initialed PTO-1449 form of record in the application in the Office Action mailed October 27, 2003.

**Foreign Priority**

The Examiner has acknowledged foreign priority in the Office Action mailed October 27, 2003.

**The Drawings**

The Examiner has accepted the drawing figures in the Office Action mailed October 27, 2003.

**Conclusion**

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E.

Amendment of January 27, 2004  
Response to Office Action of October 27, 2003

Appl. No. 09/972,963

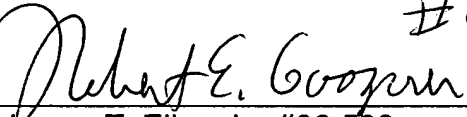
Goozner, Ph.D. (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH,

LLP

By  #42,593  
for James T. Eller, Jr., #39,538

JTE/REG/jls

P.O. Box 747  
Falls Church, VA 22040-0747  
(703) 205-8000

Attachment(s):

(Rev. 09/30/03)